IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

SALEH OSMAN ET AL

9007 6 0 834

Atty. Docket

US020557

Erial No. 10/538,632

FEB 0 9 2006

International Application No.

PCT/IB03/05938

RESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE

Commissioner for Patents, Alexandria, VA 22313

ATTENTION: APPLICATION DIVISION

RESPONSE TO NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371

Sir:

In response to the NOTIFICATION OF MISSING REQUIREMENTS mailed on December 8, 2005, enclosed is a Petition to file

Application on behalf of Co-Inventor who is Unavailable under 37

C.F.R. §1.47 and a Declaration of Facts Regarding Inventor's

Unavailability. Accordingly, the above-identified patent application is now complete.

Please charge Deposit Account No. 14-1270 any fees which may be required and credit any overpayment.

02/15/2006 MKAYPAGH 00000059 141270 10538632

01 FC:1617

130.00 DA

Respectfully submitted,

Aaron Waxler, Reg. 48,027

Attorney

(914)/333-9608

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited this date with the United States Postal Service as first-class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS

Alexandria, VA 22313-1450

ETT IN EST

LILLASO

RECEIVED

10 APR 2006

Legal Staff International Division



United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS PO. Box 1450

Alexandria, Virginia 22313-1450

U.S. APPLICATION NUMBER NO. FIRST NAMED APPLICANT		ATTY	ATTY. DOCKET NO.		
10/538,632	Saleh Osman	PH	PHUS020557 INTERNATIONAL APPLICATION NO.		
,		INTERNATIONAL AP			
	•	PCT/IB03/	05938		
24737		I.A. FILING DATE	PRIORITY DATE		
PHILIPS INTELLECTUAL PROPERTY & S	STANDARDS	12/10/2003	12/12/2002		

P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510

CONFIRMATION NO. 5395 371 FORMALITIES LETTER *OC00000017601717*

Date Mailed: 12/08/2005

NOTIFICATION OF MISSING REQUIREMENTS UNDER 35 U.S.C. 371 IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as a Designated / Elected Office (37 CFR 1.495).

Copy of the International Application fileCopy of the International Search Repor	ed on 06/10/2005 t fi <u>led on 06/10/20</u> 0	p5		Si
 Preliminary Amendments filed on 06/10 		DATE	INITIAL	
 Information Disclosure Statements filed Oath or Declaration filed on 06/10/2005 U.S. Basic National Fees filed on 06/10/2005 Priority Documents filed on 06/10/2005 	on 06/10/2005 COMPUTER 2005		EC 12 2005	
	ATTORNEY			 دی

The applicant needs to satisfy supplemental fees problems indicated below.

The following items MUST be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- Oath or declaration of the inventors, in compliance with 37 CFR 1.497(a) and (b), identifying the application by the International application number and international filing date. The current oath or declaration does not comply with 37 CFR 1.497(a) and (b) in that it:
 - is not executed in accordance with either 37 CFR 1.66 or 37 CFR 1.68.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.492(h) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fees required for this application is \$130 for a Large Entity:

\$130 Surcharge.

ALL OF THE ITEMS SET FORTH ABOVE MUST BE SUBMITTED WITHIN TWO (2) MONTHS FROM THE DATE OF THIS NOTICE OR BY 32 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

A copy of this notice **MUST** be returned with the response.

JOHN L ANDERSON

Telephone: (703) 308-9140 EXT 211

PART 1 - ATTORNEY/APPLICANT COPY

	INTERNATIONAL APPLICATION NO.	ATTY. DOCKET NO.
U.S. APPLICATION NUMBER NO.		PHUS020557
10/538,632	PCT/IB03/05938	
10/330,032		

FORM PCT/DO/EO/905 (371 Formalities Notice)



⊠Declaration Submitted With Initial Filing

Under the Paperwork Reduction Act of 1995, no persons are	• II S Patent and Trad	proved for use through 10/31/2002. OMB	OMMERCE		
	Attorney Docket Number	D			
DECLARATION FOR UTILITY OR	First Named Inventor	SALEH OSMAN			
DESIGN PATENT APPLICATION (37 CFR 1.63)	COMPLETE IF KNOWN				
	Application Number	1 .			
☑Declaration ☐Declaration Submitted OR Submitted after Initial	Filing Date				
With Initial Filing (surcharge	Group Art Unit				
Filing (37 CFR 1.16 (e)) required)	Examiner Name				

As a below named inventor, I hereby declare that:							
My residence, post office address, and citizenship are as stated below next to my name.							
Lasting Law the original first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names							
are listed below) of the subject matter wh	ich is claimed and	for which a patent is sought of	n trie invention ent	nieu.			
PRESERVING LINEARITY DYNAMICALLY ADJUSTIN	OF AN ISOL IG GAIN AND	ATUR-PREE POWE DPHASE	K AMELIE IL	N D I	Ì		
BINAMIOALLI ABOOTIII							
	(- 10)						
the specification of which	(Title of the	e Invention)					
is attached hereto							
OR was filed on (MM/DD/YYYY)		as United States App	lication Number or	PCT Internation	nal		
was filed off (WIWI/DE/1117)							
Application Number		was amended on (MM/DD/YY			(if applicable).		
I hereby state that I have reviewed and und specifically referred to above.							
I acknowledge the duty to disclose informat applications, material information which be international filing date of the continuation-i	came available bet	ial to patentability as defined tween the filing date of the pri	in 37 CFR 1.56, ind or application and t	cluding for cont the national or	inuation-in-part PCT		
	25 IIS C 110/a)-(d) or (f), or 365(b) of any fo	reign application(s) for patent, inv	entor's or plant		
breeder's rights certificate(s), or 365(a) of	any PCT internati	onal application which design	reign application(s) for patent, inv	entor's or plant		
breeder's rights certificate(s), or of any PC	T international ap	plication having a filing date	before that of the	application on	which priority is		
claimed.		Foreign Filing Date	Priority	Certified Co	py Attached?		
Prior Foreign Application Number(s)	ountry	(MM/DD/YYYY) Country	Not Claimed	YES	NO		
Additional foreign application numbers	are listed on a su	polemental oriority data shee	t PTO/SB/02B atta	ched hereto:			

[Page 1 of 2]

Burden Hour Statement: This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

PTO/SB/01 (03-01)

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION — Utility or Design Patent Application

						,		
Direct all correspondence to:	: Customer Number or Bar Code Label		•	24737*	· OR		Correspondance address	below
Philips Electronics North America Co	orporation							
Name								
P.O. BOX 3001								
Address								
BRIARCLIFF MANOR		NY				105	10	
City		State				ZIF		
U.S.A.			(914) 945	-6000	ļ	(914) 332-0615	
Country				Telepho			Fax	
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.								
NAME OF SOLE OR FIRST	INVENTOR:	□ A	petitio	n has	been fi	iled for th	is unsigned inventor	
Given Name SALEH (first and middle [if any]) SALEH Family Name OSMAN or Surname								
Inventor's Date								
NORWOOD		MA	МА		USA		GREAT BRITAIN	
Residence: City S					Country		Citizenship	
2906 VILLAGE ROAD WEST								
Mailing Address								
NORWOOD		MA			02062		USA	
City		State			Zip		Country	
NAME OF SECOND INVEN	NTOR: A	petition	has be	en file	d for th	nis unsign	ed inventor	
	RICHARD F.			Fam	ily Nam urname	ne KEEN		
	DF.Ke	en	~			Date 🗸	3/5/04	
MEDWAY WHITIN	ما انم:	MA			USA		USA	
Residence: City	RK RK	State	·		Country		Citizenship	
280 VILLAGE STREET UNIT	64 \ \ \ >	3 Cq	1	ا م	^		R.K.	
Mailing Address	(0.5	<u>> </u>	~~	· · ·				
-WEDWAY	Rik.	MA			-0205	3 RIK		
city WHitins vi		State	•		Zip	01588	Country	
				ental Add	ditional li	nventor(s) sl	heet(s) PTO/SB/02A attached	

through 10/31/2002. OMB 0651-0032 Appru

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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet Page <u>1</u> of <u>1</u>

A total according to any			otition has been fi	led fo	r this unsigned inventor	
Name of Additional Joint Inventor, if any:		1 ~ 1				
Given Name (first and middle	e [if any])	-	Fai	mily N	ame or Surname	
JAROSLAW		LUCE	K	Т		
Inventor's Signature					Date	
Residence: City CUMBERLAND	State RI	Countr	USA y		USA Citizenship	
Mailing Address 40 GREEN MEADO	W LANE					
Malling Address						
City CUMBERLAND	RI _State				USA	
Name of Additional Joint Inventor, if any:			petition has been file	d for ti	his unsigned inventor	
Given Name (first and middle [if any]) Family Name or Surname				Name or Sumame		
Inventor's Signature					Date	
Residence: City	State	Count	ry		Citizenship	
Mailing Address						
Mailing Address						
City	State	Zlp		Co	untry	
Name of Additional Joint Inventor, if any	:	ΠA	petition has been file	ed for	this unsigned inventor	
Given Name (first and middle [if any])			Family Name or Surname			
Inventor's Signature					Date	
Residence: City	ence: City State C				Citizenship	
Mailing Address						
Mailing Address						
City	State		Zip	ending	Country g upon the needs of the individual case. /	

Burden Hour Statement: This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE to a collection of information unless it contains a valid OMB control number.

Under the Paperwork Reduction Act of 1995, no persons are require

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

⊠Declaration Submitted With Initial Filing

OR

□Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

red to respond to a collection of in	formation unless it contains a valid OMB control named:
Attorney Docket Numb	DUULC020557
First Named Inventor	SALEH OSMAN
	MPLETE IF KNOWN
Application Number	1
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:							
My residence, post office a	ddress, and citizenship are	e as stated below next to r	ny name.				
I believe I am the original, first are listed below) of the subject	and sole inventor (if only one i	name is listed below) or an ori or which a patent is sought on	ginal, first and joint the invention entitl	inventor (if plural ed:	names		
DDESERVING LINE	ARITY OF AN ISOLA	ATOR-FREE POWER	RAMPLIFIER	BY	1 1		
DYNAMICALLY AD	JUSTING GAIN AND	PHASE					
					11		
	(Title of the	Invention)					
the specification of which	(This of the	,			1		
is attached hereto					1		
OR was filed on (MM/DD/Y	YYY)	as United States Appl	ication Number or I	PCT International			
		l was amended on (MM/DD/YY	YY) .	(if	applicable).		
Application Number I hereby state that I have review		at af the above identified spe	cification, including	the claims as am	ended		
hereby state that I have review specifically referred to above.	ved and understand the conter	its of the above recommend			-tion in nort		
specifically referred to above. I acknowledge the duty to discle applications, material informations.	ose information which is mater	ial to patentability as defined i	in 37 CFR 1.56, inc or application and t	luding for continu- he national or PC	ацоп-ш-ран Г		
applications, material information	of William in part application						
I hereby claim foreign priority b	enefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any fo ional application which design					
hereby claim foreign priority of breeder's rights certificate(s), of States of America, listed below breeder's rights certificate(s), of	and have also identified below	w, by checking the box any to plication having a filing date	before that of the	application on whi	ch priority is		
claimed.	of or any i or internet		Priority	Certified Copy	Attached?		
Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Not Claimed	YES	NO		
Number (5)							
			N DTO/SB/02B atta	ched hereto:			
Additional foreign applica	ition numbers are listed on a s	upplemental prionty data snee	SI F I O/GB/025 alla				

[rage | O| 2]

Burden Hour Statement: This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

PTO/SB/01 (03-01)

Approved for use through 10/31/2002. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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DECLARATION — Utility or Design Patent Application

Direct all correspondence to: Customer Num or Bar Code La		*24	737*	OR	· 🗵	Correspondance address below
Philips Electronics North America Corporation						
Name						
P.O. BOX 3001						
Address	 _				10510	
BRIARCLIFF MANOR	NY			1	10510 ZIP	
City	State					14) 332-0615
U.S.A.		1	4) 945-6000		, ,	ax
Country			lephone			
I hereby declare that all statements made herein of my obelieved to be true; and further that these statements we punishable by fine or imprisonment, or both, under 18 U application or any patent issued thereon.	S.C. 1001 and	that su	ch willful falso	stateme	ents may	ents and the like so made are y jeopardize the validity of the unsigned inventor
NAME OF SOLE OR FIRST INVENTOR:	L AP	euuoi	i ilas been			
Given Name SALEH (first and middle [if any])			Family Na or Surnan		SMAN	
Inventor's Signature				Date	e 	1
NORWOOD	MA		USA			GREAT BRITAIN
Residence: City	State		Cou	Country Citizenship		Citizenship
2906 VILLAGE ROAD WEST						
Mailing Address						1
NORWOOD	MA		020	62		USA
City	State		Zip	Zip Country		Country
	A petition h	as be	en filed for	this ur	nsigne	d inventor
Given Name RICHARD F. (first and middle [if any])			Family N	ame	KEEN/	
(instantinuole in any)						
Inventor's Signature				Da	te	· · · · · · · · · · · · · · · · · · ·
MEDWAY	МА		บร	Α		USA
Residence: City State			Co	Country Citiz		Citizenship
280 VILLAGE STREET UNIT G1						
Mailing Address						
	MA		02	053		USA
MEDWAY	State		Zi	o		Country
City Additional inventors are being named on the hereto.		ippleme			or(s) sh	eet(s) PTO/SB/02A attached



U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet Page 1 of 1

Name of Additional Joint Inventor, If any:	☐ A petition has been filed for this unsigned inventor					
Given Name (first and middle	[if any])	Family Name or Surname				
JAROSLAW		LUCEK				
Inventor's Signature & Jawaslaw	duck		メ /2 -0 f-03 Date			
Residence: City CUMBERLAND SERVICE SER	State VC	Country	USA Citizenship			
Mailing Address 40 GREEN MEADON	W LANE 307	TOWER LN				
Malling Address						
CITY GUMBERLAND G. REENSBORO	State NC	22864 ZIP 27410	USA Country			
Name of Additional Joint Inventor, if any:		☐ A petition has been filed	for this unsigned inventor			
Given Name (first and middle	(if any))	Family Name or Surname				
Inventor's Signature			Date			
Residence: City	State	Country	Citizenship			
Mailing Address						
Mailing Address						
City	tate	Zip	Country			
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor				
Given Name (first and middle	; [if any])	Family Name or Surname				
Inventor's Signature			Date			
Residence: City	State	Country	Citizenship			
Mailing Address						
Mailing Address						
City	State	Zip	Country			

Burden Hour Statement: This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re Application of

Atty. Docket

SALEH OSMAN ET AL

PHUS020557

Serial No. 10/538,632

Filed:

June 10, 2005

Title:

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER

BY DYNAMICALLY ADJUSTING GAIN AND PHASE

Commissioner for Patents Alexandria, VA 22313-1450

PETITION TO FILE APPLICATION ON BEHALF OF CO-INVENTOR WHO IS UNAVAILABLE UNDER 37 C.F.R. §1.47

Sir:

Koninklijke Philips Electronics, N.V., the owner (by assignment and operation of law) of the invention embodied in the above-referenced patent application, hereby petitions to file the accompanying application on behalf of Saleh Osman. Mr. Osman is a co-inventor of the present application. Mr. Osman conceived the subject matter of this invention while employed by Koninklijke Philips Electronics, N.V.

As more fully set forth in the accompanying "Declaration of Facts Regarding Inventor's Unavailability," several unsuccessful attempts have been made to locate and contact Mr. Osman (e.g., certified mailings, multiple telephone calls on multiple occasions, attempts to email, etc.). Therefore, Koninklijke Philips Electronics, N.V., on behalf of Mr. Osman hereby petitions the Patent Office, pursuant to 37 C.F.R. § 1.47, to allow Koninklijke Philips Electronics, N.V. to file this application on Mr. Osman's behalf.

As per 37 CFR 1.47(a) and 35 U.S.C. 116, second paragraph, all available joint inventors are required to file an application "on behalf of" themselves and on behalf of a joint inventor who "cannot be found or reached after diligent effort" or who refuses to "join in an application."

Additionally, according to 35 U.S.C. 111(a) and 115, an application deposited in the U.S. Patent and Trademark Office pursuant to 37 CFR 1.47(a) must meet the following requirements:

- A) All the available joint inventors must (1) make oath or declaration on their own behalf as required by 37 CFR 1.63 or 1.175 (see MPEP § 602, § 605.01, and § 1414) and (2) make oath or declaration on behalf of the nonsigning joint inventor as required by 37 CFR 1.64. An oath or declaration signed by all the available joint inventors with the signature block of the nonsigning inventor(s) left blank may be treated as having been signed by all the available joint inventors on behalf of the nonsigning inventor(s), unless otherwise indicated.
- (B) The application must be accompanied by proof that the nonsigning inventor (1) cannot be found or reached after diligent effort or (2) refuses to execute the application papers. See MPEP § 409.03(d).
- (C) The last known address of the nonsigning joint inventor must be stated. See MPEP § 409.03(e).

With respect to 37 CFR 1.47(a)(A), enclosed please find an executed declaration by Richard F. Keenan and Jaroslaw Lucek—the available joint inventors. With respect to 37 CFR 1.47(a)(B), the enclosed declaration of facts regarding inventor's unavailability provides proof the nonsigning inventor cannot be found or reached after diligent effot. Finally, with respect to 37 CF 1.47(a)(C), Mr. Osman's last known address is 2906 Village Road West, Norwood, MA 02062.

Respectfully submitted,

Aaron Waxler, Reg.No. 48, 027

Attorney

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re Application of

Atty. Docket

SALEH OSMAN ET AL

PHUS020557

Serial No.

Filed:

CONCURRENTLY

Title:

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER

AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE

Commissioner for Patents Alexandria, VA 22313-1450

DECLARATION OF FACTS REGARDING INVENTOR'S UNAVAILABILITY

I Dicran Halajian hereby declare that:

I prepared the above-referenced patent application.

A copy of the patent application, drawings, declaration, and assignment were emailed to the co-inventors for review and comment. However, Mr. Saleh Osman is no longer employed by Koninklijke Philips Electronics, N.V., and all attempts to contact Mr. Osman have failed.

Multiple attempts were made to call Mr. Osman at the last known phone number. Multiple messages were left on an answering machine. No return call was received from Mr. Osman.

On December 12, 2002, October 24, 2003 and March 5, 2004, the application packet, including declaration and assignment, were sent to Mr. Osman's last known address via Federal Express. Mr. Osman has not returned the documents to Koninklijke Philips Electronics, N.V.

Mr. Osman's last known address is 2906 Village Road West, Norwood, MA 02062.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statement and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

6/9/05 Date

Dicran Halajian, Reg. No. 39,703



Richard Keenan 10/17/2006 07:11 AM To Korne Vennema/SVL/SC/PHILIPS@PHILIPS

CC Jarek Lucek/SVL/SC/PHILIPS@PHILIPS Peter Zawilski/SVL/IPS/PHILIPS@PHILIPS

bcc

Subject Re: US020555 Patent Application titled, "PRESERVING

LINEARITY OF AN ISOLATOR-FREE POWER...and US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...

Classification Unclassified

Peter,

I also do not have his contact information.

Rich

Richard Keenan

RFID Applications Engineer - Identification

BU A&I - Sales & Marketing NXP Semiconductors

2178 Mendon Rd., Suite 300

Cumberland, RI 02864 USA

Tel: +1 401 305 5059

Mob: +1 508 509 1000 Fax: +1 401 305 5060

email: richard.keenan@nxp.com

PHILIPS SEMICONDUCTORS has become NXP SEMICONDUCTORS !!!

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Korne Vennema

PHILIPS

Kome Vennema 10/17/06 09:20 AM To Jarek Lucek/SVL/SC/PHILIPS@PHILIPS

cc Peter Zawilski/SVL/IPS/PHILIPS@PHILIPS
Richard Keenan/SVL/SC/PHILIPS@PHILIPS

Subject Re: US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...and

US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...

Classification Unclassified

Peter,

Unfortunately I do not have his contact information either.

Korné Vennema Sr. Marketing Application Engineer NXP Semiconductors



2178 Mendon Road, Suite 300 Cumberland, RI 02864 USA

Office Phone: (401) 305-5051, Mobile: (401) 578-0463

Lab Phone: (401) 305-5058 (no voice mail)

Mobile Holland: +31-6-13660653 e-mail: korne.vennema@nxp.com

Jarek Lucek

Jarek Lucek

10/16/06 08:47 PM

To Peter Zawilski/SVL/IPS/PHILIPS@PHILIPS

cc Korne Vennema/SVL/SC/PHILIPS@PHILIPS Richard Keenan/SVL/SC/PHILIPS@PHILIPS

Subject Re: US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER ... and

US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...

Classification Unclassified

Hi, Peter,

I don't have contact info for Saleh. Shortly after filing the patents we have let him go.

Korne Vennema or Rich Keenan might have his contact info. I've copied them both on ths email.

Regards,

Jarek Lucek NXP Semiconductors - founded by Philips 508-446-6739 cell http://www.semiconductors.com/products/rf/index.html

All transactions for the purchase of NXP Semiconductors' products are subject to NXP Semiconductors' general terms and conditions of commercial sale. These are published at: http://www.nxp.com/profile/terms/index.html

Peter Zawilski

To Jarek Lucek/SVL/SC/PHILIPS@PHILIPS

Subject US020555 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER ... and US020557 Patent Application titled, "PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER...

Classification Unclassified

Peter Zawilski 10/16/06 03:14 PM

Dear Jarek::

I telephoned you earlier in the day and left a message on your voicemail.

I am the Patent Agent managing the above cases, you originally had worked with attorneys in Philips, Briarcliff Manor, New York offices (under Philips IP&S). These cases had been filed in the US Patent Office in December 2003.

I am trying to locate co-inventor Saleh Osman. Apparently, during the filing of the US application he did not sign the Oath & Declaration. Without his signature, the cases will not move forward. You and other co-inventor Richard Keenan had signed.

As of this morning, I have not been able to locate Mr. Osman. Would you happen to have a current E-mail address and telephone number of Mr. Osman?

I appreciate your help.

Hope to hear from you in a day or so.

Kindest regards,

Peter Z

Peter S. Zawilski Patent Agent

NXP Semiconductors Intellectual Property Department

Visitor's address: 1130 Ringwood Court; Mail Stop SJ41, San Jose, CA 95131 USA

Courier address: 1140 Ringwood Court; Mail Stop SJ41

San Jose, CA 95131 USA

Mail address: 1109 McKay Drive; Mail Stop SJ41, San Jose, CA 95131 USA

Phone: +1 408 474 9063 Facsimile: +1 408 474-9082

Main Phone: (408) 434-3000 Email: peter.zawilski@philips.com Intranet: pww.ips.philips.com Internet: www.nxp.com

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Peter Zawilski

Patent Agent

Intellectual Property Department **NXP** Semiconductors Tel: +1 408 474 9063, Fax: +1 408 474 9082 1109 McKay Drive, M/S-41, San Jose, CA 95131 USA peter.zawilski@nxp.com, www.nxp.com

October 19, 2006

Mr. Saleh Osman 2906 Village Road West Norwood, MA 02062

VIA EXPRESS MAIL

Philips Filing No.: US 020557; US Application Serial No. 10/538,632 filed 10-JUN-2005

Titled: Preserving Linearity of an Isolator-Free Power Amplifier by Dynamically Adjusting

Gain and Phases

Dear Saleh:

The above-name patent application was filed in the United Patent Office. Your colleagues Richard Keenan and Jaroslaw Lucek had signed the required papers for completing the filing. However, your signature is necessary for the case to move forward.

I have enclosed a copy of the as filed application for your review. Please sign, date, and return the Oath & Declaration to me at your earliest convenience. A prepaid return envelope has been enclosed. Also, please fax back a copy of both pages to me at (408) 474-9082.

NXP formerly Philips Semiconductors, appreciates your support in protecting its valuable IP assets.

If you have any questions, please feel free to get in touch with me.

Very truly yours,

Peter Zawilski Patent Agent (408) 474-9063

Exhibita DECLARATION FOR Attorney Docket Number US 020557 UTILITY OF DESIGN Osman, Saleh First Named Invent PATENT APPLICATION COMPLETE IF KNOWN (37 CFR 1.63) **Application Number** 10/538,632 Declaration **Declaration** 06/10/2005 Filing Date Submitted with Submitted after Initial Initial Filing OR Filing (surcharge **Group Art Unit** (37 CFR 1.16(e)) required) Examiner Name As a below named inventor, I hereby declare that: My residence, post office address, and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: Preserving Linearity of an Isolator-Free Power Amplifier by Dynamically Adjusting Gain and Phase (Title of the Invention) the specification of which: is attached hereto

was filed on (MM/DD/YYYY) 06/10/2005 as United States Application Number or PCT International Application Number 10/538,632 and was amended on (MM/DD/YYYY) 06/10/2005 (if applicable).

hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

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Prior Foreign Application Numbers(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Co Yes	py Attached? No
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Additional foreign application numbers are listed on a supplemental priority data sheet attached hereto:





DECLARATION ---- Utility or Design Patent Application

Direct all correspondence to:	er Number 24	738	AND/OR	Corres	spondence address below	
PHILIPS ELECTRONICS NORTH A Intellectual Property & Stand		RPORA	ATION		,	
Address 1109 McKay Drive, M/S-41SJ					Acceptance of the second secon	
_{city} San Jose	State	Califo	ornia		_{ZIP} 95131	
Country U.S.A	Telephone	(408)	474-907	'3	FAX (408) 474-9082	
hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may eopardize the validity of the application or any patent issued thereon.						
NAME OF SOLE OR FIRST INVENTOR	: 🗆	A pet	ition has be	en filed for this	s unsigned inventor	
Given Name SALEH (first & middle [if any])			Family N or Surna	lame OSMA	AN	
Inventor's Signature					Date	
Norwood Residence: City	MA State		U.S Coun		Great Britain Citizenship	
2906 Village Road West Mailing Address						
Norwood city	MA State		ZIP 0	2062	U.S.A. Country	
NAME OF SECOND INVENTOR:		A peti	ition has be	en filed for this	s unsigned inventor	
Given Name RICHARD F. (first & middle [if any])			Family N or Surna	^{ame} KEEN	AN	
Inventor's Signature					Date	
Whitinsville Residence: City	MA State		U.S Coun		U.S.A Citizenship	
103 Carole Lane Mailing Address	10000				TO MESTIVE TO THE PERSON OF TH	
Whitinsville city	MA State		O ZIP	1588	U.S.A.	
NAME OF THIRD INVENTOR:		A peti	ition has be	en filed for this	s unsigned inventor	
Given Name (first & middle [if ang)			Family Nor Surna	ame LUCE me	K	
Inventor's Signature					Date	
Greensboro Residence: City	NC State		U.S. Count		U.S.A Citizenship	
307 Tower Lane Mailing Address					1	
Greensboro _{City}	NC State		ZIP 2	7410	U.S.A. Country	
☐ Additional inventors are being named on the	B	suppler	mental Add	itional Inventor	(s) sheet(s) attached hereto.	





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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

SALEH OSMAN ET AL

US020557

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE

Commissioner for Patents Alexandria, VA 22313-1450

	CERTIFICATE OF EXPRESS MAILING
Express Mail Label No	EV 664 854 860 US
Date of DepositJune 10	2005
"Express Mail Post Office to	per and/or fee is being deposited with the United States Postal Service of Addressee" service under 37 C.F.R. 1.10 on the date indicated above nmissioner for Patents, PO Box, 1450, Alexandria, VA 22313-1450
Patti DeMichele Typed Name	Signature DM JOE

in JUN 1 0 2005

Exhibit 2

Under the Paperwork Reduction A

PTC-1390 (Rev. 02-2005)

A ed for use through 3/31/2007, OMB 0651-0021

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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displays a valid OMB control number.

TRANSMITTAL LETTENSO	THE UNITED STATES
DESIGNATED/ELECTED	OFFICE (DO/EO/US)
CONCERNING A SUBMISSIO	N UNDER 35 U.S.C. 371

ET NUMBER ATTORNEY'S

DESIGNATED/ELECTED OFFICE (DO/EO/US)		PHUS020357
	CONCERNING A SUBMISSION UNDER 35 U.S.C. 371	
INTERNATIONAL APPLICATION NO. PCT/IB2003/005938	INTERNATIONAL FILING DATE 10 December 2003	PRIORITY DATE CLAIMED 12 December 2002
TITLE OF INVENTION PRESERVING LINEARITY OF AN ISOLA		
APPLICANT(S) FOR DO/EO/US		
SALEH OSMAN, RICHARD F. KEENAN a Applicant herewith submits to the United Sta	ites Designated/Elected Office (DO/FC	D/US) the following items and other information:
	ncerning a submission under 35 U.S.C. 371	
2. This is a SECOND or SUBSEQUENT su	ubmission of items concerning a submission	n under 35 U.S.C. 371.
3. This is an express request to begin nation (5), (6), (9) and (21) indicated below.	onal examination procedures (35 U.S.C. 37	1(f)). The submission must include items
4. The US has been elected (Article 31).		
5. A copy of the International Application	n as filed (35 U.S.C. 371(c)(2))	
a. Is attached hereto (required	only if not communicated by the Internation	nal Bureau).
b.	the International Bureau.	
c. is not required, as the applic	cation was filed in the United States Receiv	ing Office (RO/US).
6. An English language translation of the	e International Application as filed (35 U.S.C	C. 371(c)(2)).
a. is attached hereto.		
b. has been previously submit	tted under 35 U.S.C. 154(d)(4).	
7. Amendments to the claims of the Inte	mational Application under PCT Article 19	(35 U.S.C. 371(c)(3))
a. are attached hereto (requir	red only if not communicated by the Interna	itional Bureau).
b. have been communicated	by the International Bureau,	
c. have not been made; howe	ever, the time limit for making such amendr	ments has NOT expired.
d. have not been made and v	MII not be made.	
8. An English language translation of th	ne amendments to the claims under PCT Ar	rticle 19 (35 U.S.C. 371(c)(3)).
9. An oath or declaration of the inventor	(8) (35 U.S.C. 371(c)(4)).	
10. An English language translation of the Article 36 (35 U.S.C. 371(c)(5)).	e annexes of the International Preliminary E	Examination Report under PCT
Items 11 to 20 below concern document(s	i) or information included:	
11. An Information Disclosure Statement	under 37 CFR 1.97 and 1.98.	
	ng. A separate cover sheet in compliance w	ith 37 CFR 3.28 and 3.31 is included.
13. A preliminary amendment.		
14. An Application Data Sheet under 37 (CFR 1.76.	
15. A substitute specification.		
16. A power of attorney and/or change of	f address letter.	
17. A computer-readable form of the sequ	uence listing in accordance with PCT Rule	13ter.2 and 37 CFR 1.821- 1.825.
18. A second copy of the published Intern	national Application under 35 U.S.C. 154(d)(4).
Europe 1	ge translation of the international applicatio	n under 35 U.S.C. 154(d)(4). PTO/SB08A; Charge Authorization; Receipt
Other items or information: Express M	Mail Certificate; 27	L 10/2000M; Charke varioussmon! veccibr

Other items or information: Confirmation Postcard,
This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering information, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mall Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Page 1 of 2

Page 1 of 2

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Approv U.S. Patent and Trademan 995, no persons are required to respond to a collection of information. PTO-1390 (Rev. 02-2005) se through 3/31/2007. OMB 0651-0021 U.S. DEPARTMENT OF COMMERCE it displays a valid OMB control number.

Under the Paperwork Reduction A ATTORNEY'S DOCKET NUMBER INTERNATIONAL APPLICATION NO. U.S. APPLICATION NO. (if known, see 37 CFR 1.5) PCT/IB2003/005938 PHUS020557 CALCULATIONS PTO USE ONLY The following fees have been submitted Basic national fee......\$300 21. 🔽 300.00 22.
Examination fee
If International preliminary examination report prepared by USPTO and all claims satisfy provisions of \$ 200.00 23. Search fee Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an \$ 400.00 All other situations......\$500 \$ 900.00 TOTAL OF 21, 22 and 23 = Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing or computer program listing filed in an electronic medium). The fee is \$250 for each additional 50 sheets of paper or fraction thereof. RATE Extra Sheets Number of each additional 50 or fraction **Total Sheets** thereof (round up to a whole number) \$ x \$250 -100 =/50 = Surcharge of \$130,00 for furnishing the oath or declaration later than 30 months from the earliest \$ claimed priority date (37 CFR 1.492(h)). NUMBER FILED NUMBER EXTRA RATE \$ CLAIMS \$ - 20 = x \$50 0.00 Total claims 17 x '\$200 \$ - 3 = 0.00 Independent claims \$360 MULTIPLE DEPENDENT CLAIM(S) (if applicable) TOTAL OF ABOVE CALCULATIONS = \$ 0.00 Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by 1/2. SUBTOTAL = \$ 900.00 Processing fee of \$130.00 for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). TOTAL NATIONAL FEE = \$ 900.00 Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied \$ 40.00 by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property TOTAL FEES ENCLOSED = \$ 940.00 Amount to be refunded: Amount to be \$ 940.00 charged: to cover the above fees is enclosed. A check in the amount of \$ in the amount of \$ 940.00 b. 🔽 Please charge my Deposit Account No. 14-1270 ___ to cover the above fees. A duplicate copy of this sheet is enclosed. c. 🗸 The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1270 . A duplicate copy of this sheet is enclosed. Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card Information should not be included on this form. Provide credit card information and authorization on PTO-2038. NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status. SEND ALL CORRESPONDENCE TO: Corporate Patent Counsel Aaron Waxler Philips Electronics North America Corporation NAME P.O. Box 3001 Briarcliff Manor, NY 10510 REGISTRATION NUMBER

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

To Commissioner For Patents Enclosed herewith is a Form PTO-1449, any required copies of documents listed thereon, and any concise explanation of their relevance is indicated below per 37 CFR 1.97.

Application Number	
Filing Date	CONCURRENTLY
First Named Inventor	SALEH OSMAN ET AL
Group Art Unit .	N/A
Examiner Name	N/A
Attorney Docket Number	US020557

X Please Account	e charge any required fee under §1.17(i) or §1.17(p) or No. 14-1270.	any other i	equired fee (exc	ept the issue fee) to	
1.	ify that these documents were first cited in any communant foreign application not more than three (3) months	nication fro	om a foreign Pate	ent Office in a	
counterr	ify that none of these documents were cited in any compart foreign application, and, to the knowledge of the undocuments was known to any individual designated in	ndersigned	after making rea	sonable inquiry, none	
☐ Appli Allowan	cant hereby petitions under §1.97(d) that this IDS be ce, pays the fee under §1.17(p) as indicated below, and	onsidered a l I certify 1	fter final Action or 2. as indicate	or Notice of ed above.	
A fee months	under §1.17(p) is not required under §1.97(c), after the date of application or RCE, because I certify I	e first Action. or 2. as in	on on the merits adicated above.	and more than (3)	
applicati	oy of the citations is not required because they were proon (or in U.S. patent application Ser. No				
A copy of the U.S. patent(s) and patent application publication(s) in all U.S. national patent applications filed after June 30, 2003, and in all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003 under 37 CFR 1.491(b), are not required.					
A cor designat	A concise explanation of the relevance of each non-English document, as understood by the individual designated in §1.56(c) most knowledgeable about the contents, is enclosed per §1.98(a)(3).				
The concise explanation of the relevance of any non-English document, as understood by the individual designated in §1.56(c) most knowledgeable about the contents, is that the document is/was:					
図 cited in the specification or considered in drafting the specification of this application;					
previously submitted or cited in the parent application (or in a related patent application Ser. No					
cited a	as an "X" or "Y" document in a foreign Patent Office s which report is also enclosed.	earch repor	t in a foreign co	unterpart application, a	
	SIGNATURE OF APPLICANT, ATTORNEY, O	OR AGENT RI	EQUIRED		
Name (Print Type)	Aaron Waxler /	Registration N	o. (Attorney/Agent)	48,027	
Signature	412	Date	Cella	106	



PTO/SB/08A (08-03)
Approved Is through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1

Complete if Known					
Application Number					
Filing Date	Concurrently				
First Named Inventor	SALEH OSMAN ET AL				
Art Unit	N/A				
Examiner Name	N/A				
Attorney Docket Number	US020557				

Examiner	Cite	Document Number	Publication Date	T DOCUMENTS Name of Patentee or	Pages, Columns, Lines, Where
Initials*	No.1		MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
		Number-Kind Code ^{2 (# snown)}			- I igures Appeel
		^{US-} 5,423,082	06-06-1995	CYGAN	
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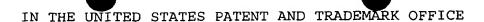
		FORE	IGN PATENT DOCU	MENTS		
Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered, include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. Applicant is to place a check mark here if English language

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



In re Application of

Atty. Docket

SALEH OSMAN ET AL

US020557

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE

Commissioner for Patents Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please add the following paragraph before the first paragraph beginning at page 1, line 1:

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. provisional application serial no. 60/432,897 filed December 12, 2002, which is incorporated herein by reference.

The invention relates to an isolator-free power amplifier circuit typically used in wireless communication devices which preserves linearity of the power amplifier under varying loads. More particularly, linearity is preserved by dynamically adjusting the gain by changing the input bias of active devices of the power amplifier circuit, and/or by dynamically adjusting the phase of a pre-amplified signal.

REMARKS

By means of the present amendment, the specification has been amended to include a claim of priority.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Respectfully submitted,

Aaron Waxler, Reg. 48,027

Attorney

(914) 333-9608

PTO/SB/01 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
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DECLARATION FOR UTILITY OR
DESIGN
PATENT APPLICATION
(37 CFR 1.63)

⊠Declaration OR Submitted With Initial Filing

□ Declaration Submitted after Initial

Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number		PH	July 20557		
First Named Inventor		SA	LEH OSM	AN	
CO	MPLI	ETE	IF KNOWN		
Application Number		1			
Filing Date					
Group Art Unit					
Examiner Name					/

As a below named inve	ntor, I hereby declare tha	at:						
My residence, post office address, and citizenship are as stated below next to my name.								
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names								
are listed below) of the subject matter which is claimed and for which a patent is sought on the Invention entitled:								
PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE								
the specification of which	(Title of th	e Invention)						
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was filed on (MM/DD/	was filed on (MM/DD/YYYY) as United States Application Number or PCT International							
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I hereby state that I have revier specifically referred to above.	wed and understand the conte	nts of the above identified spe	ecification, including	g the claims as a	mended			
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.								
I hereby claim foreign priority to breeder's rights certificate(s), States of America, listed below breeder's rights certificate(s), claimed.	or 365(a) of any PCT internat v and have also identified belo	ional application which design w, by checking the box any for	nated at least one preign application(s	country other the) for patent, inve	an the United into sor plant			
Prior Foreign Application		Foreign Filing Date	Priority	Certified Cop	y Attached?			
Number(s)	Country	(MM/DD/YYY) Country	Not Claimed	YEŞ	NO			
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[Page 1 of 2]

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Inventor's Signature						Date	
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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

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Filing

Declaration
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(37 CFR 1.16 (e))

required)

Attorney Docket Number	er PHUS020557	
First Named Inventor	SALEH OSMAN	
COM	PLETE IF KNOWN	
Application Number	1	
Filing Date		
Group Art Unit		
Examiner Name		

As a below named inventor, I hereby declare that:								
My residence, post office address, and citizenship are as stated below next to my name.								
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:								
PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE								
the specification of which	(Title of th	e Invention)						
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I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.								
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Inventor's Signature				Date		
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PATENT COOPERATION TREAT



From the INTERNATIONAL BUREAU

WAXL

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:

KONINKLIJKE PHILIPS ELECTRONICS N.V. c/o Biren, Steven R. P.O. Box 3001 Briarcliff Manor, NY 10510-8001 ETATS-UNIS D'AMERIQUE

Date of mailing (day/month/year) 24 June 2004 (24.06.2004)

Applicant's or agent's file reference PHUS020557WO

IMPORTANT NOTICE

International application No. PCT/IB2003/005938 International filing date (day/month/year) 10 December 2003 (10.12.2003) Priority date (day/month/year) 12 December 2002 (12.12.2002)

Applicant

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KONINKLUKE PHILIPS ELECTRONICS N.V. et al

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this notice:

AU, AZ, BY, CH, CN, CO, DZ, EP, HU, JP, KG, KP, KR, MD, MK, MZ, RU, TM, US

In accordance with Rule 47.1(c), third sentence, those Offices will accept the present notice as conclusive evidence that the mmunication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:

AE, AG, AL, AM, AP, AT, BA, BB, BG, BR, BZ, CA, CR, CU, CZ, DE, DK, DM, EA, EC, EE, EG, ES, FI, GE, GD, GE, GH, GM, HR, ID, IL, IN, IS, KE, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MG, MN, MW, MX, NI, NO, NZ, OA, M, PG, PH, PL, PT, RO, SC, SD, SE, SG, SK, SL, SY, TJ, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW

The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

- 3. Enclosed with this notice is a copy of the international application as published by the International Bureau on 24 June 2004 (24.06.2004) under No. WO 2004/054097
- 4. TIME LIMITS for filing a demand for international preliminary examination and for entry into the national phase

The applicable time limit for entering the national phase will, subject to what is said in the following paragraph, be 30 MONTHS from the priority date, not only in respect of any elected Office if a demand for international preliminary examination is filed before the expiration of 19 months from the priority date, but also in respect of any designated Office, in the absence of filling of such demand, where Article 22(1) as modified with effect from 1 April 2002 applies in respect of that designated Office. For further details, see PCT Gazette No. 44/2001 of 1 November 2001, pages 19926, 19932 and 19934, as well as the PCT Newsletter, October and November 2001 and

In practice, time limits other than the 30-month time limit will continue to apply, for various periods of time, in respect of certain designated or elected Offices. For regular updates on the applicable time limits (20, 21, 30 or 31 months, or other time limit), Office by Office, refer to the PCT Gazette, the PCT Newsletter and the PCT Applicant's Guide, Volume II, National Chapters, all available from WIPO's Internet site, at http://www.wipo.int/pct/en/index.html.

For filing a demand for international preliminary examination, see the PCT Applicant's Guide, Volume I/A, Chapter IX. Only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination (at present, all PCT Contracting States are bound by Chapter II).

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The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland

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PC JUN 3 0 2004

Form PCT/IB/308 (April 2002)

(19) World Intellectual Property Organization

International Bureau



(43) International Publication Date 24 June 2004 (24.06.2004)

PCT

(10) International Publication Number WO 2004/054097 A1

(51) International Patent Classification⁷: H03G 3/20, H03F 1/02

H03F 1/56,

(21) International Application Number:

PCT/IB2003/005938

(22) International Filing Date:

10 December 2003 (10.12.2003)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

60/432,897

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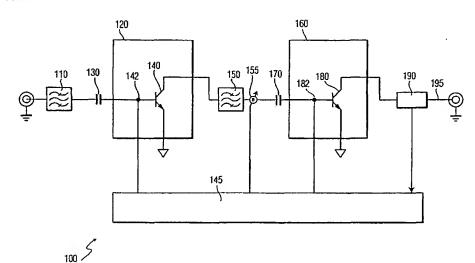
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- (84) Designated States (regional): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW). Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM). European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

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[Continued on next page]

(54) Title: PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE



(57) Abstract: An amplifier circuit (100) includes a driver stage (120) with at least an active device (140) for pre-amplification and output of a pre-amplified signal; and an output stage (160) with at least an active device (180) for further amplification of the pre-amplified signal and output of an amplified signal. A phase shifter (155) shifts the phase of the pre-amplified signal. A detector (190) measures levels of forward and reflected parts of the amplified signal, and a gain and phase control circuit (145) independently and selectively controls and adjusts the phase shifter (155) for optimal amplifier performance and minimal difference between the forward and reflected signals. The gain and phase control circuit also independently and selectively controls and modifies the gain of the active devices (140, 180) of the driver and output stages (120, 160) as a function of the levels of the forward and reflected signals to substantially maintain constant linearity of the amplifier circuit (100) with load variations.

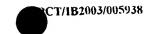
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PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE

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The invention relates to an isolator-free power amplifier circuit typically used in wireless communication devices which preserves linearity of the power amplifier under varying loads. More particularly, linearity is preserved by dynamically adjusting the gain by changing the input bias of active devices of the power amplifier circuit, and/or by dynamically adjusting the phase of a pre-amplified signal.

Power amplifiers are used in transmitters to amplify signals, such as radio frequency (RF) signals. Such power amplifiers are included in transmitters of wireless communication devices, such as mobile telephones. The power amplifier typically provides an amplified RF signal to an antenna for transmission over the air.

RF antennas as for instance applied in mobile phones, operate in strongly varying environments, resulting in a varying antenna input impedance, a VSWR (Voltage Standing Wave Ratio) of 4:1 is not uncommon. Especially at high output levels, this may result in a severe distortion of for instance a CDMA (code division multiple access), TDMA (time division multiple access), Edge or W-CDMA modulated carrier signal having a nonconstant envelope.

The conventional solution to protect the power amplifier of a cellular phone against antenna mismatch conditions to preserve linearity is to use an isolator, such as a circulator, placed between the power amplifier and the output load, such as the antenna, to limit the effects of load impedance variation on the performance of the power amplifier. The circulator secures proper 50 Ohm loading of the power amplifier under antenna mismatch conditions by dissipating the reflected power in the isolator or in a third circulator port termination. Directivity in the power flow is created by ferromagnetic material.

The above aspects of the state of the art are described in more detail with reference to Fig. 1 which shows a basic block diagram of an arrangement 10 used for a power source 12 isolated with a circulator 14 from a mismatched antenna 16. A current source 18 and its impedance Z₀ represent an ideal power source (RF-transistor) 12. A matching circuit 20 is

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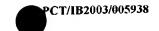
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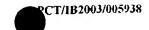


connected between the antenna 16 and power source 12, with another terminal 22 connected to ground.

Part of the power P_{inc_circ} from the matching circuit 20 to the circulator 14 is delivered as P_{inc_ant} to the antenna 16 where some power is reflected back P_{refl_ant} to the circulator 14. Thanks to the circulator 14, the reflected power P_{refl_ant} from the antenna 16 is not reflected towards the source 12, but dissipated into the circulator load P_{diss}. Consequently, the reflected power P_{refl_circ} from the circulator 14 and the reflected power P_{refl_source} from the matching circuit 20 towards the source 12 are zero. This avoids extremes that would occur when incident and reflected waves add up in-phase. However, since it is desired to preserve power amplifier linearity and maintain Prad constant (under control of field strength indication at the base station), then the incident power P_{inc_source} from the source 12 has to be increased, thus increasing power dissipation, to overcome reflection losses resulting in enhanced signal voltage and current at the source 12. Thus, the circulator 14 only partly preserves power amplifier linearity under antenna mismatch conditions. In addition, power dissipation and consumption remains high thus requiring battery charging and decreasing battery life of the mobile phone as well as decreasing efficiency.

It is desirable to remove the isolator or circulator 14 connected to the antenna 16. However, removal of the isolator allows load impedance variations to detrimentally affect the performance, e.g., linearity, of the power amplifier. Accordingly, there is a need to have a power amplifier circuit where the isolator is removed yet the performance and linearity of the amplifier is preserved despite load impedance variations.

According to the invention, linear power output of a power amplifier is substantially maintained constant despite load variations and having no isolator connected to the load. This is achieved by dynamically adjusting the gain of active devices and phase of signals in an isolator-less power amplifier circuit as a correction scheme for linearity under predetermined load mismatch conditions. Thus, linear output power is kept unchanged for a predetermined load delta across the dynamic range of operation, without substantially decreasing efficiency. More particularly, linearity is substantially maintained constant despite load variations by independently and selectively adjusting the gain of the active devices of driver and output stages as a function of the levels of the forward and reflected output signals. Further, the phase of a pre-amplified signal is independently and



selectively adjusted as a function of the levels of the forward and reflected output signals to substantially maintain constant linearity of amplifier circuit with load variations.

In one embodiment according to the present invention, an amplifier circuit for preserving linearity of an amplifier is provided. The amplifier circuit may be used in wireless communication devices, for example. The amplifier circuit includes a driver stage with at least an active device for pre-amplification and output of a pre-amplified signal; and an output stage with at least an active device an active device for further amplification of the pre-amplified signal and output of an amplified signal. A phase shifter shifts the phase of the pre-amplified signal. A detector measures levels of forward and reflected parts of the amplified signal, and a gain and phase control circuit independently and selectively controls and adjusts the phase shifter for optimal amplifier performance and maximum difference or ratio between the forward and reflected signals. The gain and phase control circuit also independently and selectively controls and modifies the gain of the active devices of the driver and output stages as a function of the levels of the forward and reflected signals to substantially maintain linearity of amplifier circuit with load variations.

In another embodiment according to the present invention, a method for substantially preserving linearity of an amplifier under varying loads is provided. The method includes measuring levels of forward and reflected signals at the amplifier output; and adjusting the phase of a pre-amplified signal for optimal amplifier performance and maximum difference or ratio difference between the forward and reflected signals as a function of the measured levels, such as the difference or ratio of the measured forward and reflected signals. The method further includes independently and selectively adjusting the gain of the active devices of the driver stage and/or output stage, such as by selectively adjusting the DC bias at the input of the active devices, as a function of the levels of the forward and reflected signals to substantially maintain linearity of amplifier circuit with load variations.

Further features and advantages of the invention will become more readily apparent from a consideration of the following description.

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The accompanying drawings specify and show preferred embodiments of the invention, wherein like elements are designated by identical references throughout the drawings; and in which:

Fig. 1 shows a prior art block diagram of a power source isolated with a circulator from a mismatched antenna;

Fig. 2 shows a wireless communication system according to the present invention;

Fig. 3 shows an isolator-free amplifier circuit according to the present invention;

Fig. 4 shows a flow chart of a method for preserving performance, e.g., linearity, of an isolator-free amplifier circuit according to the present invention; and

Fig. 5 shows a summarized flow chart of the method for preserving performance, e.g., linearity, of an isolator-free amplifier circuit according to the present invention.

The invention, together with attendant advantages, will be best understood by reference to the following detailed description of the preferred embodiment of the invention, taken in conjunction with the accompanying drawing.

An amplifier circuit for use in wireless communication devices for example is described where, illustratively, an RF power amplifier is used in RF antenna circuits. In the following description, numerous specific details are set forth, such as specific type and number of transistors, in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known circuits have not been set forth in detail in order to not unnecessarily obscure the present invention.

The wireless communication device may be for example a mobile cellular or cordless telephone, pager, an Internet appliance or other consumer devices, and is typically part of a communication system. Fig. 2 shows a wireless communication system, such as a mobile telephone system 40 comprising a primary or base station (BS) 50 and a plurality of secondary or mobile stations (MS) 60. The BS 50 comprises a network controller 52, such as a computer, coupled to a transceiver 54 which is in turn coupled to radio transmission means such as an antenna 56. A connection means such as a wire 58 couples the controller 52 to a public or a private network.

Each MS 60 comprises a processor 62 such as a micro-controller (μ C) and/or a digital signal processor (DSP). Typically, the DSP processes voice signals, while the μ C

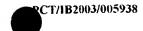
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manages operation of the MS 60. The processor 62 is coupled to a transceiver means 64 coupled to radio transmission means, e.g., an antenna 66. A memory 68, such as an EPROM and RAM, is coupled to the processor 62 and stores data related to operation and configuration of the MS 60. Communication from the BS 50 to MS 60 takes place on a downlink channel 72, while communication from the MS 60 to BS 50 takes place on an uplink channel 74. The MS 60 also includes a user interface such as a keyboard and a screen, as well as a microphone coupled to the transmit branch or section of the transceiver 64 and a speaker coupled to the receiver section of the transceiver 64.

The transmit section of the transceiver 64 transmits signals over the uplink channel 74, which the receive branch of the transceiver 64 receives signals over the downlink channel 72. The transceiver 64 includes a selection means to selectively couple a power amplifier (PA) of the transmit section or a low noise amplifier (LNA) of the receive section to the antenna 66. Illustratively, the selection means includes a duplexer or bandpass filters tuned to the transmit and receive frequency ranges, respectively. As is well known in the art, the transceiver 64 also includes other circuits such as a down converter for converting the received radio frequency (RF) signals to intermediate frequency and/or baseband signals, and demodulator/decoder in the receive branch. By contrast, the transmit branch of the transceiver 64 includes an up converter and a modulator/encoder. Converters that convert between analog and digital formats are also typically present in the transceiver 64.

Fig. 3 shows an embodiment of an amplifier circuit 100 according to the present invention which is illustratively used as a power amplifier circuit to amplify RF signals in wireless communication devices. For example, the amplifier circuit 100 is part of the transceiver 64 of the MS 60 shown in Fig. 2, and more particularly, in the transmit branch of the transceiver 64. Typically, the input of the amplifier circuit is coupled to a modulator and receives modulated RF signals for amplification. The amplifier output is coupled to a load, such as the antenna 66, where the amplified RF signals are transmitted over the air on the uplink channel 74 for example.

As shown in Fig. 3, the amplifier circuit 100 comprises an input match circuit 110 for buffering the input of the amplifier circuit 100 and matching its input impedance with the output impedance of the circuit coupled thereto, such as a modulator. The output of the input match circuit 110 is coupled to a driver stage 120 through at least one direct current (DC) blocking capacitor 130. The signal to be amplified, such as a modulated signal, is

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provided by the input match circuit 110 to the capacitor 130, which substantially blocks DC components and provides a signal substantially without a DC offset to the driver stage 120.

The driver stage 120 comprises at least one active device, such as a transistor 140, which receives the substantially DC-free signal from the capacitor 130 for preamplification to a first level. Illustratively, the pre-amplification transistor is a bipolar transistor, such as an NPN transistor 140 having a base 142 coupled to the capacitor 130. The base 142 is further independently coupled to a gain and phase control circuit 145 for a proper DC biasing signal. This allows the control circuit 145 to control, e.g., adjusts the DC bias at the input of the transistor 140. The emitter of the transistor 140 is coupled to ground, while the output or collector of the transistor 140 is coupled to an inter-stage match circuit 150 for buffering and impedance matching between the driver stage 120 and the input 182 of an output stage 160.

The pre-amplified signal from the driver stage 120 is provided to the input 182 of the output stage 160 through the inter-stage match circuit 150, a phase shifter 155 which shifts the phase of the pre-amplified signal, and at least one DC blocking capacitor 170 for substantially blocking DC signals present in the pre-amplified and phase-shifted signal, similar to the DC blocking capacitor 130.

The output stage 160 is similar to the driver stage 120 and also comprises at least one transistor 180 which receive the substantially DC-free signal from the capacitor 170 for amplification to the output level. Illustratively, the output transistor 180 is a bipolar transistor, such as an NPN transistor having a base coupled to the capacitor 170. The base 182 of the output transistor 180 is further coupled to the control circuit 145 for providing the proper DC biasing signal the output transistor 180. The emitter of transistor 180 is coupled to ground, while the output or collector of the transistor 180 is directly or indirectly coupled to the load without any isolation therebetween. Further, the emitter area of each active device 140, 180 is selected such that optimum performance is achieved for a given load, inter-stage and source conditions.

In addition to being coupled to the inputs 142, 182 of the transistors 140, 180, the control circuit 145 is also coupled to a control port of the phase shifter 155. Accordingly, the control circuit 145 is configured to provide control signals for independently and selectively controlling the phase shifter 155 and transistors 140, 180. This allows the bias

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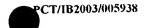
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control circuit 145 to independently and selectively adjust the amount phase shifting of the pre-amplified signal and the DC bias at the input transistors 140, 180, thus adjusting the amplification or gain of the driver and output stages 120, 160.

By way of example, suppose a power amplifier is to deliver 30 dBm of output power to a 50 ohm load. If the power amplifier's final stage's output has peak voltage swing of 1.4 volts for linear operation, then a loss-less impedance matching network separating load and power amplifier must have an impedance transformation ratio of 51:1.

Consider a worst case mismatch condition over all phases of a constant VSWR. The two impedance extremes are high and low loads. In the former case, large voltage swings develop across the output of the final stage causing non-linearity in the form of clipping due to the onset of high AC impedance. In the later case, the demand for output current elevates due to the onset of low AC impedance. By monitoring the incident and reverse power levels, a measurement of the impedance condition is obtained as shown in block 200 of Fig. 4. Next in block 210, the impedance level or mismatch is checked and if a normal or matched level is obtained, then normal matched operation is continued in block 220. If the impedance level or mismatch is not normal, then it is determined in block 230 whether the difference or ratio of the measured forward and reflected signals is high, indicating a relatively high forward signal, or low indicating a relatively low forward signal. Next, in block 240, the phase shifter and the input DC bias of each driver and output transistor are independently and selectively adjusted in one direction or the other, depending on whether the ratio measured in block 230 was high or low. Next, the impedance condition is remeasured by returning to block 200 and the operations are repeated until a matched level is obtained in block 210 and normal matched operation is continued in block 220. The monitoring and measurement of the impedance in block 200 are continuously or intermittently checked and adjustments are made, if needed, to arrive to the matched condition of block 220.

A detector, such as a power detector 190, is also coupled to the output of transistor 180 for detecting the level, e.g., the power level, of the amplified RF signal at the output of the output stage 160. The power detector 190 is in turn coupled to the control circuit 145. The output 195 of the amplifier circuit 100 is coupled to an antenna without an isolator therebetween.

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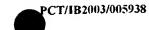
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The power detector 190 provides the control circuit 145 a measure of the forward and reflected output power of the amplifier circuit 100. As a function of the forward and reflected power levels, the control circuit 145 independently and selectively controls the phase shifter 155 and each of transistor 140, 180 of the driver and output stages 120, 160 to substantially maintain the optimum performance and constant linearity of the amplifier circuit 100 despite variations in the impedance of the load connected to the output 195 of the amplifier circuit 100. For example, in response to the difference between the forward and reflected power level in response to the difference between the forward and reflected power level, the control circuit 145 independently and selectively controls the phase shifter 155 and changes the DC bias on the input e.g., base 142, 182, of each driver and output transistor 140, 160. This substantially maintains linear output power despite load variations without significantly modifying the output stage of the power amplifier circuit.

As is well known by one skilled in the art, the changes in the forward and reflected power levels measured by the power detector 190 are related to changes in the load impedance, e.g., the impedance of the antenna 66 shown in Fig. 2. In particular, for a load impedance substantially matched to the output impedance of the output of the amplifier circuit 100, the ratio or the difference between the forward and reflected power levels is high, while it is low for substantially mismatched impedances. U.S. Patent No. 5,423,082, which is incorporated herein by reference in its entirety, discloses a transmitter that includes a closed loop feedback to compensate for varying antenna loads without an isolator, which is accomplished by taking the reflected output energy into account to maintain a constant overall loop gain by adjusting the gain of variable gain stages.

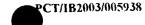
Control circuits are also well known in the art, such as the control circuit disclosed in U.S. Patent Nos. 5,442,322 and 5,712,593 which are incorporated herein by reference in its entirety. In U.S. Patent No. 5,442,322, a bias control circuit compares a bias control voltage with a value indicative of the current in an active device and provides a control signal to the control terminal of the active device to control the operating point thereof. The bias point of a power amplifier is similarly controlled in U.S. Patent No. 5,712,593 by a control circuit in response to comparing a reference value to a filtered portion of the RF output signal. Changing the amplifier bias point limits the effect of the load impedance variation on the amplifier performance. U.S. Patent No. 6,064,266, which is incorporated herein by reference in its entirety, is also related to limiting the effect of the load

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impedance variation on the amplifier performance, which is achieved by modifying the RF output signal path, instead of the DC bias, by switching in a resistor in parallel with the output impedance when a threshold detector detects variations in the load impedance above a predetermined value. Phase shifters are also well known in the art, as disclosed in U.S. Patent No. 4,312,032, which is incorporated herein by reference in its entirety.

The control circuit 145 of the present amplifier circuit 100 may include a processor or a comparator for comparing the values of forward and reflected power levels measured by the power detector 190 with at least one threshold value. Based on the comparison, the control circuit 145 selectively and independently controls modifies the DC levels at the inputs 142, 182 of the transistors 140, 180, as well as controlling the phase shifter 155 to change the phase of the pre-amplified signal as necessary, namely, as a function of the levels of the forward and reflected signals, to substantially maintain constant the linearity of the amplifier circuit 100 with load variations.

Fig. 5 shows a flow chart 300 of a method for preserving performance of an isolator-free amplifier circuit according to the present invention. In block 310, the power detector measures the forward and reflected power levels at the output of the amplifier circuit and provides this information to the control circuit 145. In response to the measured forward and reflected power levels, such as their difference or ratio values, in block 320, the control circuit 145 selectively and independently controls the phase shifter 155 to change the phase of the pre-amplified signal, and/or modifies the gain, e.g., by changing the base DC bias, of the input and/or output transistors 140, 180, as a function of the measured forward and reflected power levels to substantially maintain optimal performance and constant linearity of the amplifier circuit 100 with load variations.

While the present invention has been described in particular detail with reference to specific exemplary embodiments thereof, it should also be appreciated that numerous modifications and changes may be made thereto without departing from the broader and intended spirit and scope of the invention as set forth in the claims that follow. The specification and drawings are accordingly to be regarded in an illustrative manner and are not intended to limit the scope of the claims which follow.

CLAIMS:

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1. An amplifier circuit comprising:

a driver stage having at least a first active device which receives a signal for preamplification and outputs a pre-amplified signal;

a phase shifter which adjusts a phase of said pre-amplified signal and outputs a phase-shifted signal;

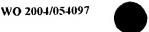
an output stage having at least a second active device which receives said phaseshifted signal for further amplification and output of an amplified signal;

a detector which measures levels of forward signal and reflected signal of said amplified signal; and

a control circuit which controls said phase shifter in response to said levels of forward signal and reflected signal to substantially maintain linearity of said amplifier circuit with load variations.

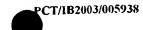
- 2. The amplifier circuit of claim 1, wherein said output stage is coupled to a load without an isolation device between said output stage and said load.
- 3. The amplifier circuit of claim 1, wherein said control circuit modifies a gain of at least one of said at least first active device and said at least second active device to substantially maintain said linearity of said amplifier circuit with said load variations.
 - 4. The amplifier circuit of claim 1, wherein said control circuit independently controls said at least first active device and said at least second active device.
 - 5. The amplifier circuit of claim 1, wherein said control circuit independently controls said phase shifter, said at least first active device and said at least second active device to substantially maintain said linearity of said amplifier circuit with said load variations.
 - 6. The amplifier circuit of claim 1, wherein said at least first active device and said at least second active device are NPN transistors.

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- The amplifier circuit of claim 1, further comprising an input match circuit coupled 7. between an input of said amplifier circuit and said driver stage for matching an input impedance of said amplifier circuit to an output impedance of a device coupled to said input.
- The amplifier circuit of claim 7, further comprising at least one capacitor coupled 8. between said input match circuit and said driver stage.
- The amplifier circuit of claim 1, further comprising at least one capacitor coupled 10 9. between an input of said amplifier circuit and said driver stage.
 - The amplifier circuit of claim 1, further comprising an inter-stage match circuit 10. coupled between an output of said driver stage and an input of said phase shifter.
 - The amplifier circuit of claim 10, further comprising at least one capacitor coupled 11. between said phase shifter and said output stage.
- The amplifier circuit of claim 1, further comprising at least one capacitor coupled 12. between said phase shifter and said output stage. 20
 - A wireless communication device comprising the amplifier circuit of claim 1. 13.
 - An amplifier circuit comprising: 14.
- a driver stage having at least a first active device which receives a signal for pre-25 amplification and outputs a pre-amplified signal;
 - a phase shifter which adjusts a phase of said pre-amplified signal and outputs a phase-shifted signal;
- an output stage having at least a second active device which receives said phaseshifted signal for further amplification and output of an amplified signal; 30
 - a detector which measures levels of forward signal and reflected signal of said amplified signal; and





a control circuit which independently and selectively controls switching said phase shifter, said at least first active device, and said at least second active device as a function of said levels of forward signal and reflected signal to substantially maintain linearity of said amplifier circuit with load variations.

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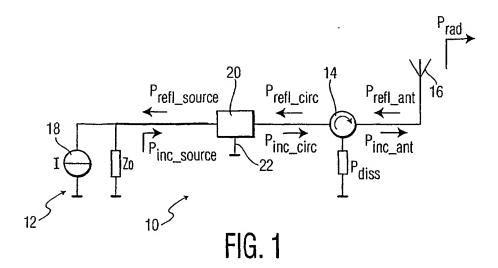
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- 15. A method for substantially maintaining linearity of an amplifier circuit with variations of a load coupled to an output of said amplifier circuit comprising: measuring levels of forward signal and reflected signal at said output; and modifying a phase shifter to change a phase of an output signal of said amplifier circuit as a function of said levels to substantially maintain linearity of said amplifier circuit with load variations.
- 16. The method of claim 15, wherein said modifying act further modifies a first gain of a first active device of a driver stage, and a second gain of a second active device of an output stage of said amplifier circuit in response to said levels to substantially maintain said linearity.
- 17. The method of claim 16, wherein said modifying act independently and selectively modifies said phase shifter, said first gain and a second gain.

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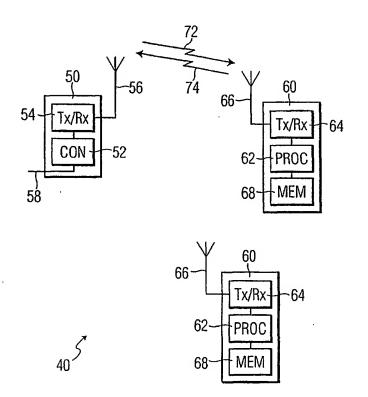
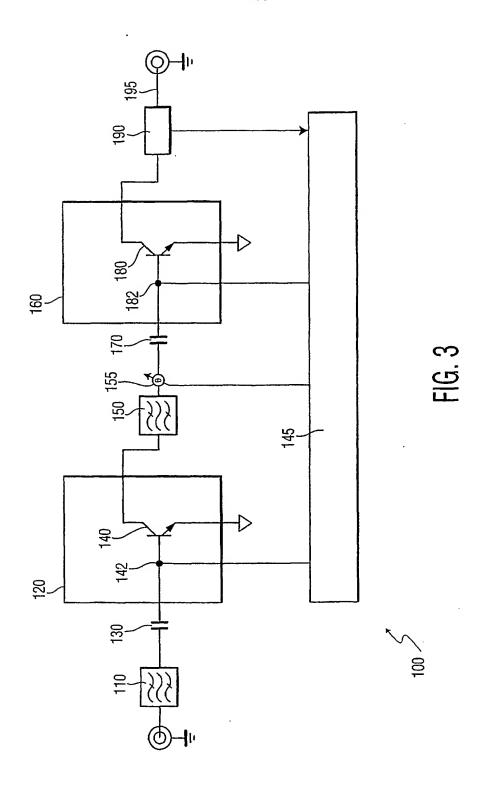


FIG. 2

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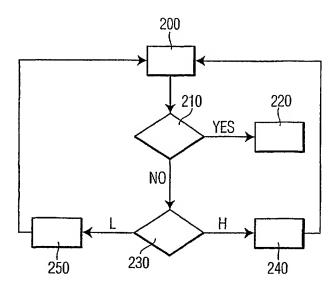
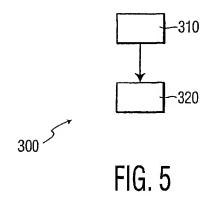


FIG. 4



INTERNATIONAL SEARCH REPORT

PCT/203/05938

A. CLASSII IPC 7	FICATION OF SUBJECT M. H03F1/56 H03G3/20 H03F1/02								
According to	International Patent Classification (IPC) or to both national classifica	tion and IPC]						
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C. DOCUMENTS CONSIDERED TO BE RELEVANT									
Category °	Citation of document, with indication, where appropriate, of the rele	evant passages	Relevant to daim No.						
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Furtl	ner documents are listed in the continuation of box C.	Y Patent family members are listed	in annex.						
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		EARCH REPO				
Patent document cited in search report		Publication date		Patent family member(s)		Publication date
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IN THE FED STATES PATENT AND TRADE

In re Application of

Atty. Docket

SALEH OSMAN ET AL

US020557

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

PRESERVING LINEARITY OF AN ISOLATOR-FREE POWER AMPLIFIER BY DYNAMICALLY ADJUSTING GAIN AND PHASE

Commissioner for Patents Alexandria, VA 22313-1450

AUTHORIZATION PURSUANT TO 37 CFR 1.136(a)(3) AND TO CHARGE DEPOSIT ACCOUNT

Sir:

The Commissioner is hereby requested and authorized to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time.

Please charge any additional fees which may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

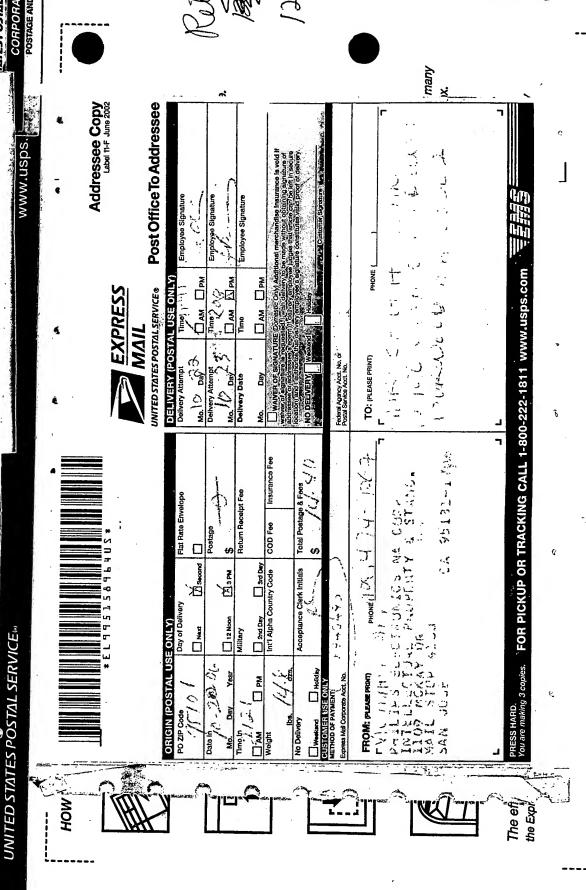
Respectfully submitted,

Aaron Wakler, Reg. 48,02

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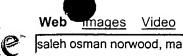
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